**DAILY ASSESSMENT FORMAT**

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| **Date:** | **03-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **Digital Design using HDL** | **USN:** | **4AL17EC035** |
| **Topic:** | **1.EDA Playground Online Compiler**  **2.EDA Playground Tutorial Demo Vedio**  **3.How to Download and install Xilinx Vivado Design Suite**  **4.Vivado Design Suite for implementation for HDL code** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**          **Verilog code for INVERTER** |
| **Verilog code for RIPPLE\_CARRY\_COUNTER**      **TASK 3: Implement 4 to 1 MUX using two 2 to 1 MUX using Structural Modelling style and test the module in online/offline compiler** |

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| **Date:** | **03-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **PYTHON** | **USN:** | **4AL17EC035** |
| **Topic:** | **Section 30** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **AFTERNOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**    **Application 8: Scrape Real Estate Property Data from the Web** |

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